ABSTRACT OF THE DISCLOSURE

A data processing system having shared memory accessible through a transaction-based bus mechanism. A plurality of system components, including a central processor, are coupled to the bus mechanism. The bus mechanism includes a cache coherency transaction within its transaction set. The cache coherency transaction comprises a request issued by one of the system components that is recognized by a cache unit of the central processor as an explicit command to perform a cache coherency operation. The transaction further comprises a response issued by the central processor indicating status of the cache coherency operation.

BOULDER:0041815.03